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FIG. 1A

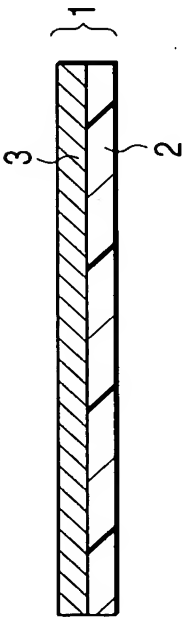


FIG. 1B

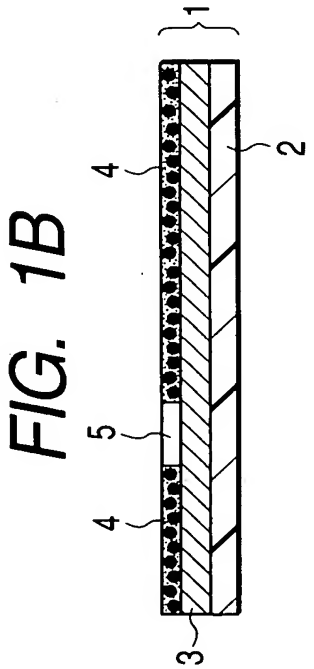


FIG. 1C

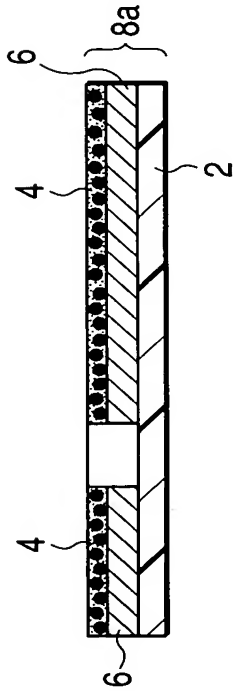


FIG. 1D

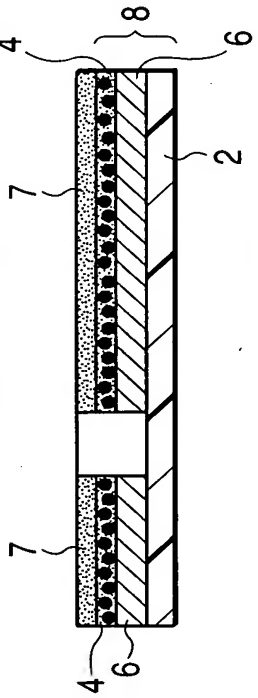


FIG. 1E

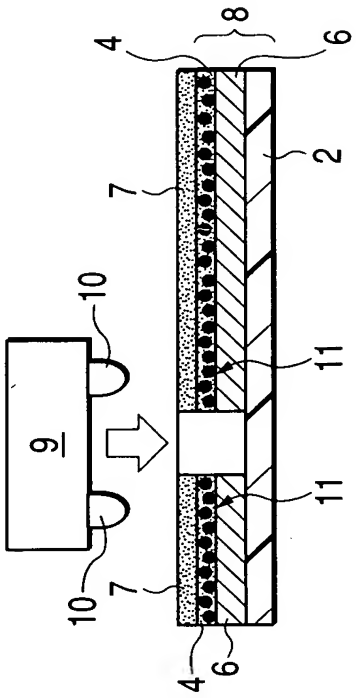


FIG. 1F

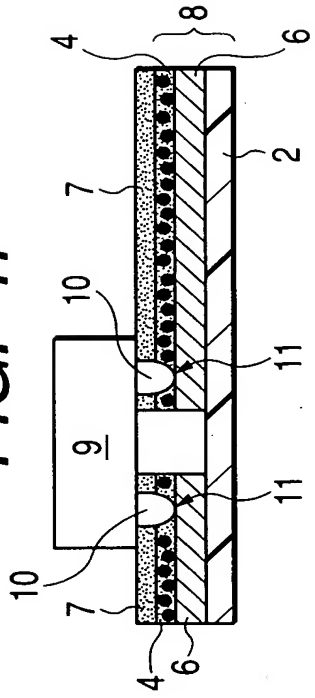


FIG. 2A

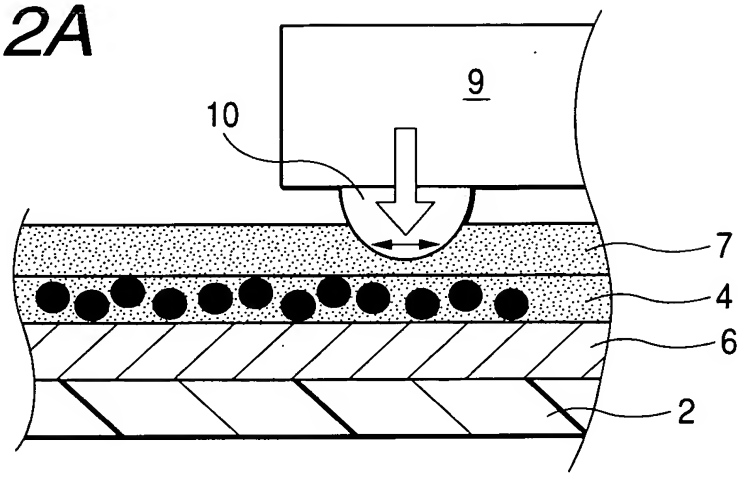


FIG. 2B

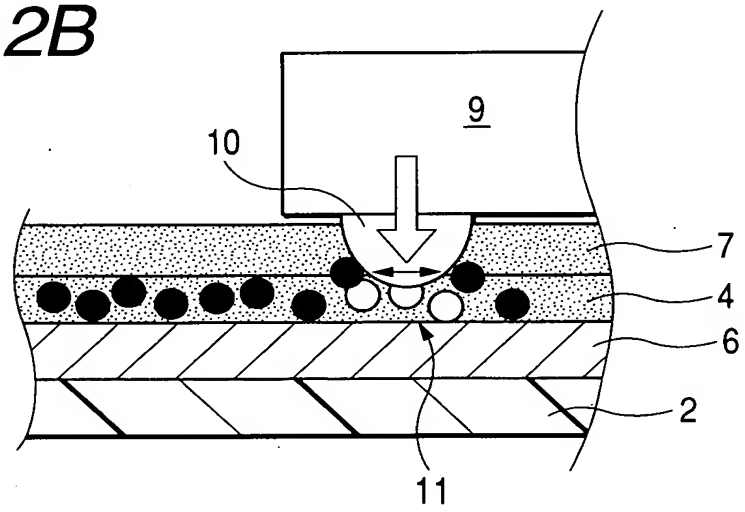


FIG. 2C

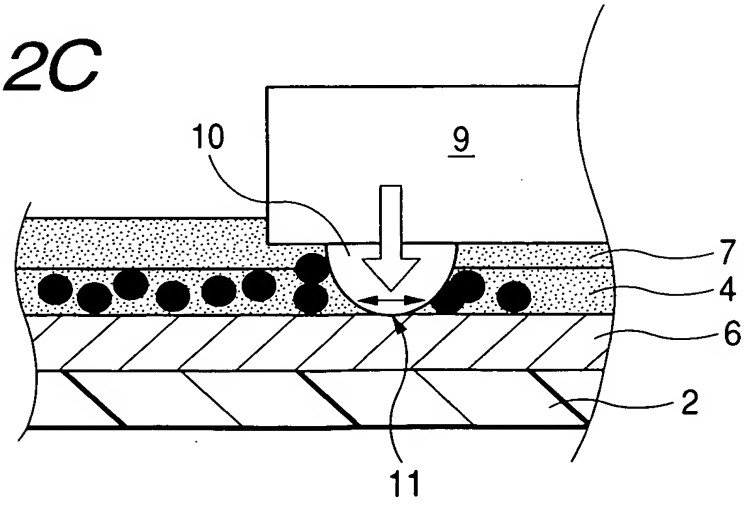


FIG. 3A

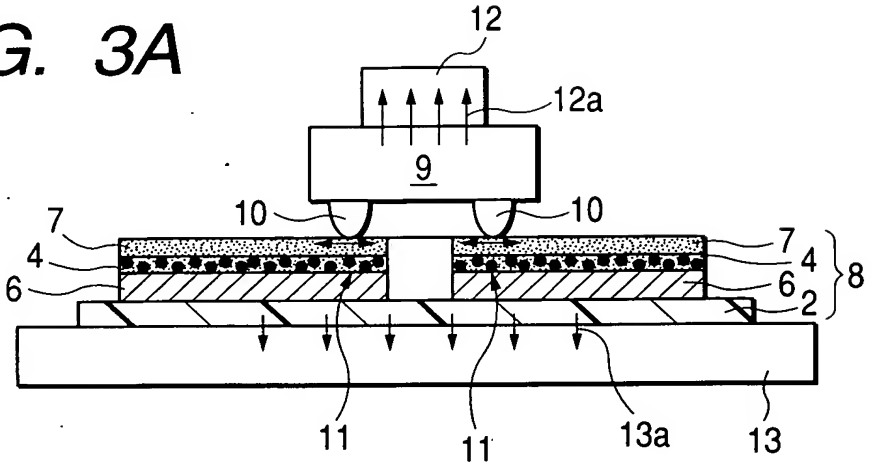


FIG. 3B

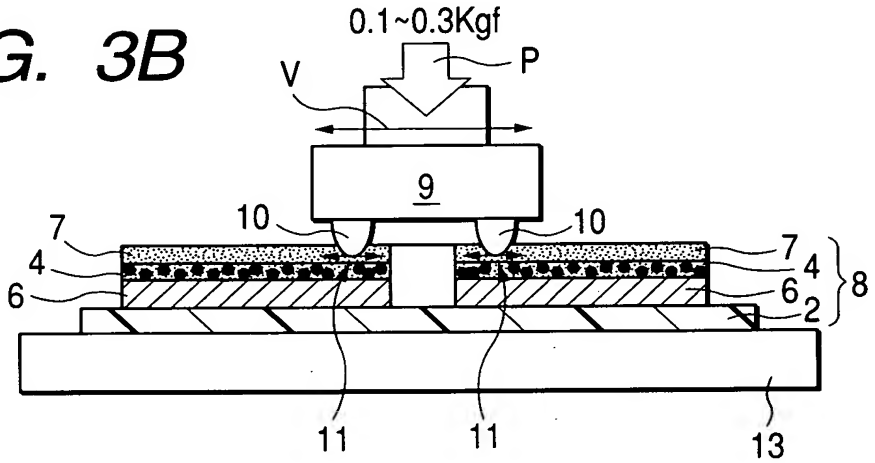


FIG. 3C

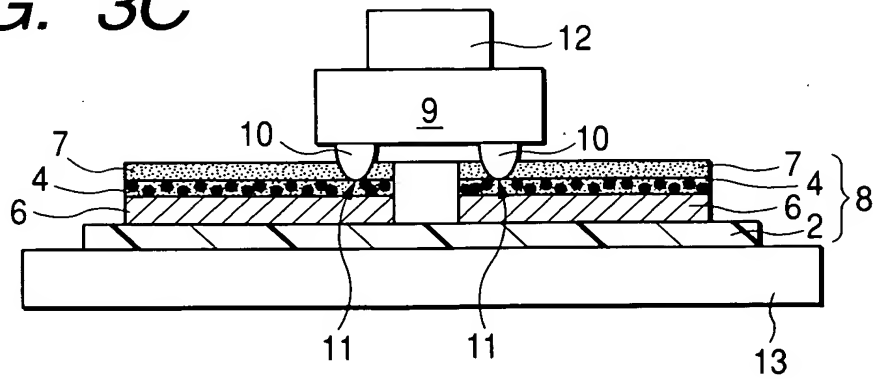


FIG. 4A

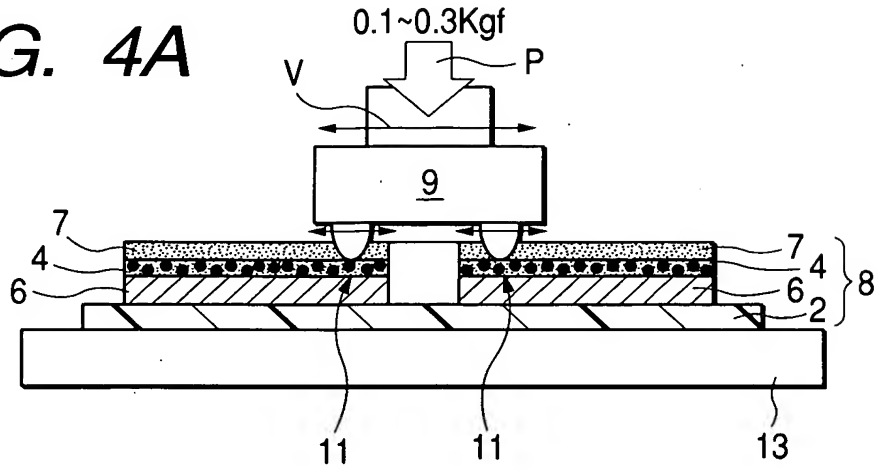


FIG. 4B

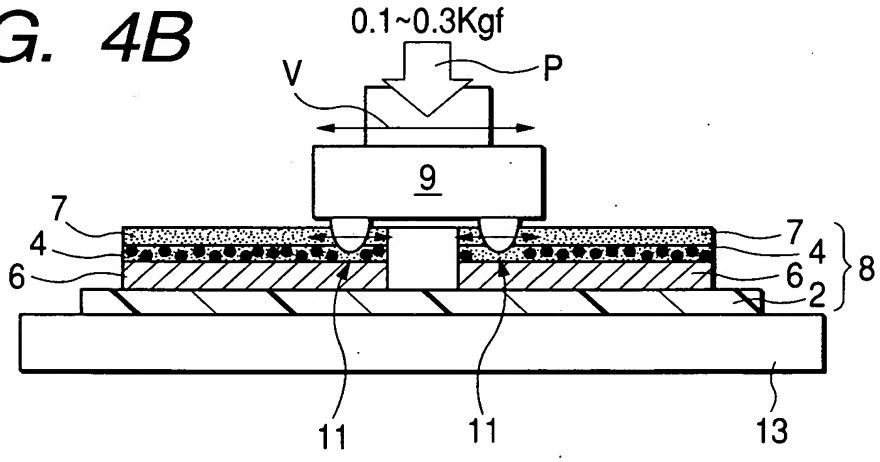


FIG. 4C

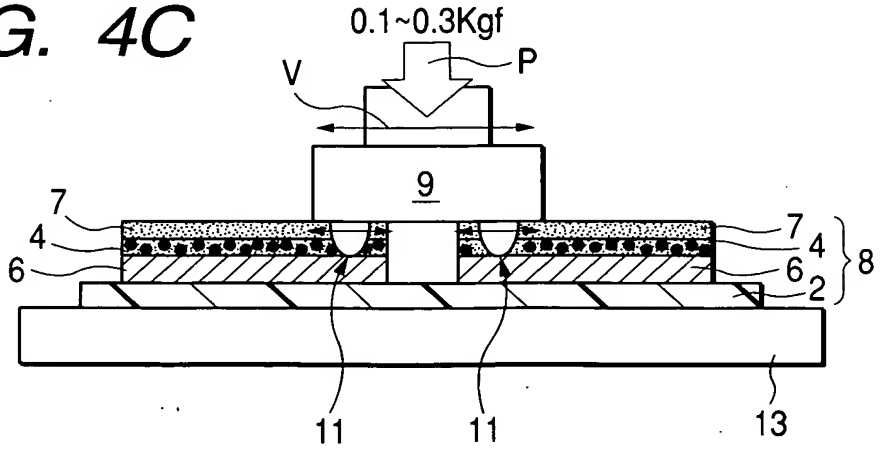


FIG. 5

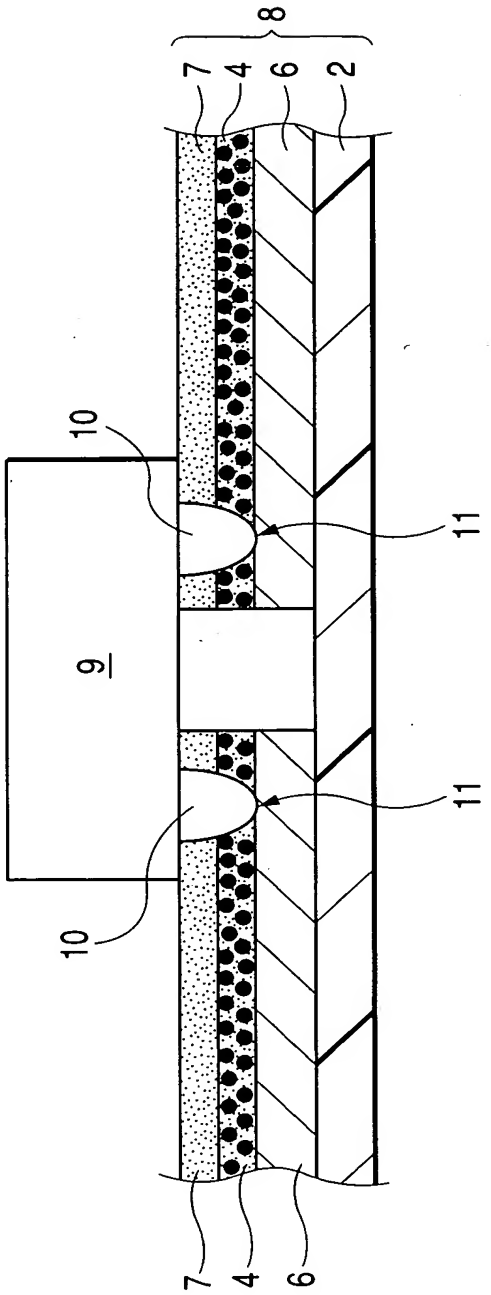


FIG. 6A

SEMICONDUCTOR MOUNTING METHOD	ULTRASONIC BONDING	EMBODIMENT
BONDING STRENGTH	200 ~ 250	1400 ~ 1700

FIG. 6B

SEMICONDUCTOR MOUNTING METHOD	THIRD METHOD OF THE RELATED ART	EMBODIMENT
SHORT-CIRCUIT FAILURE OCCURRENCE RATIO	5.0%	0.0%

FIG. 7A

SiO_2 PARTICLES	NONE	PRESENT (EMBODIMENT)
SEMICONDUCTOR CHIP BONDING FAILURE (100 TESTS)	96.0%	0.0%

FIG. 7B

SiO_2 PARTICLES	1 ~ 2μm	3 ~ 4μm (EMBODIMENT)
SEMICONDUCTOR CHIP BONDING FAILURE (100 TESTS)	50.0%	0.0%

FIG. 8

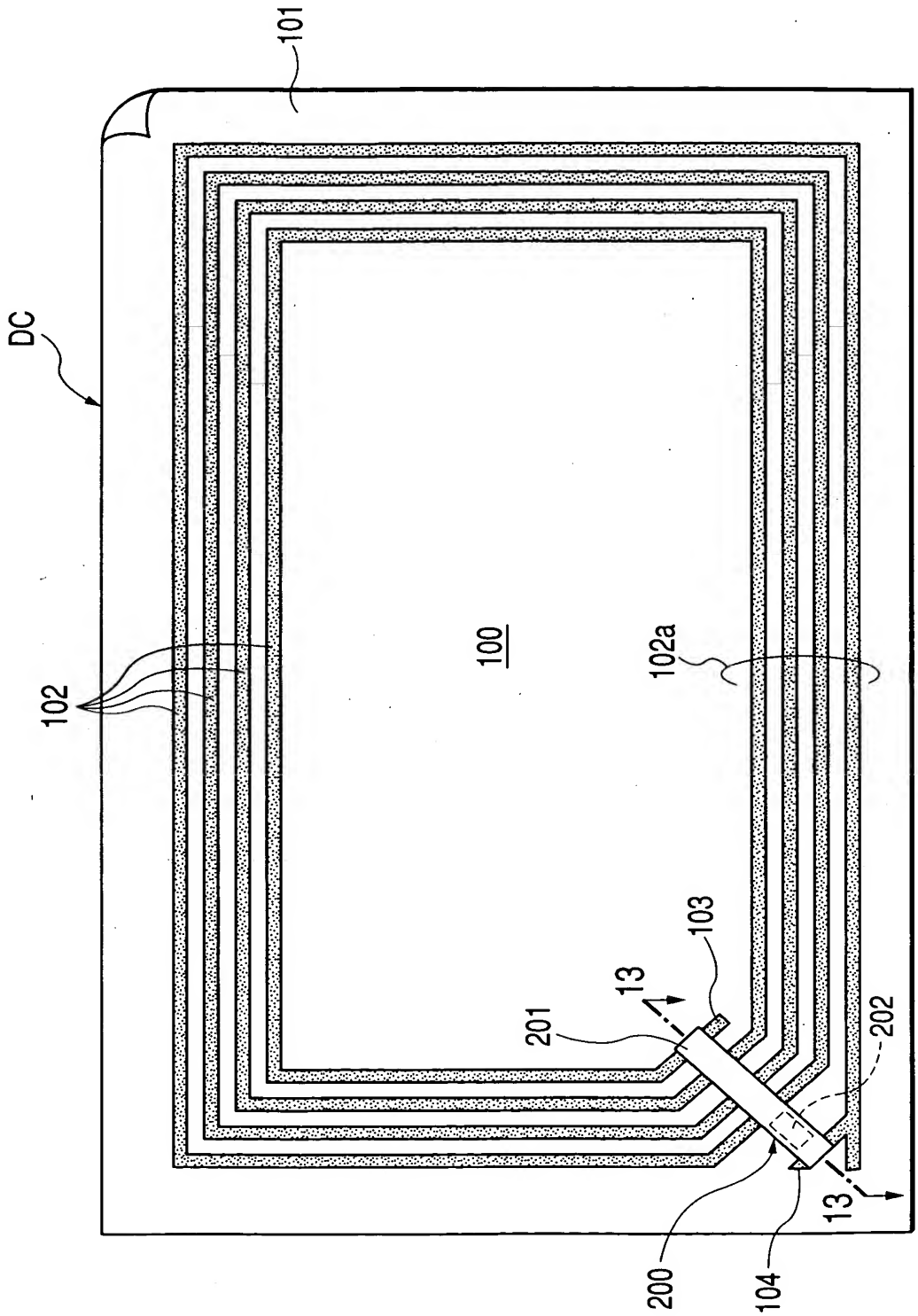


FIG. 9

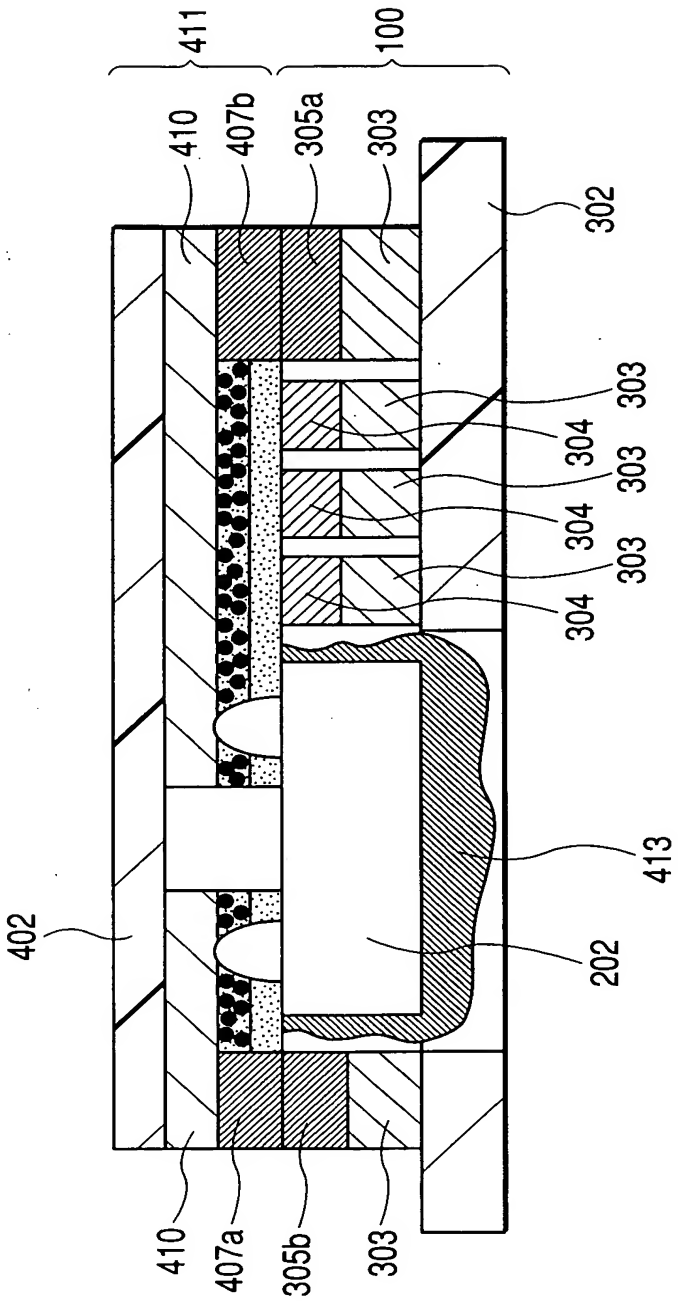

411
100
410
407b
305a
303
302
303
304
303
304
303
304
413
402
202
410
407a
305b
303

FIG. 10A

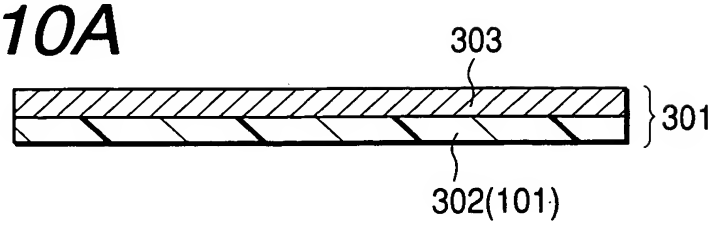


FIG. 10B

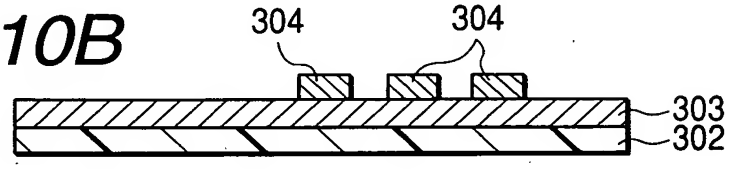


FIG. 10C

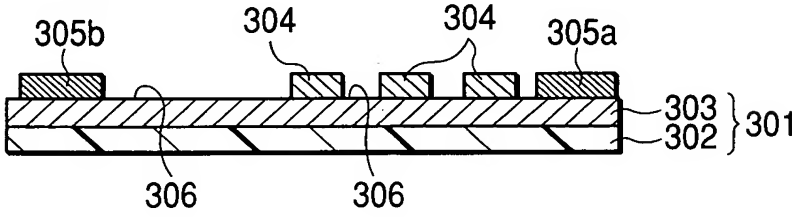


FIG. 10D

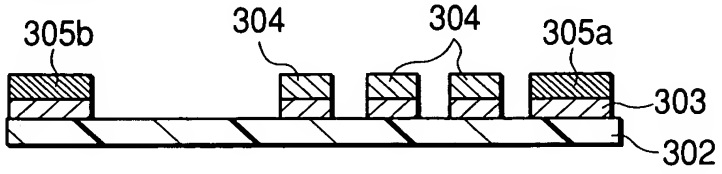


FIG. 10E

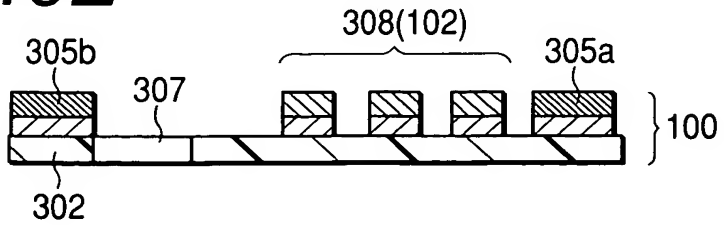


FIG. 11A

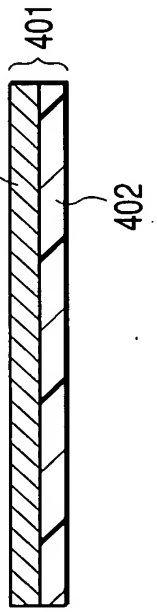


FIG. 11B

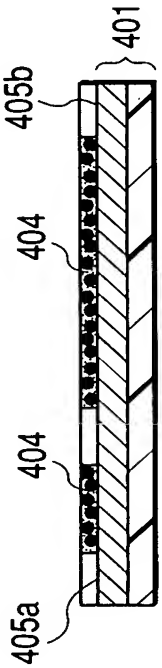


FIG. 11C

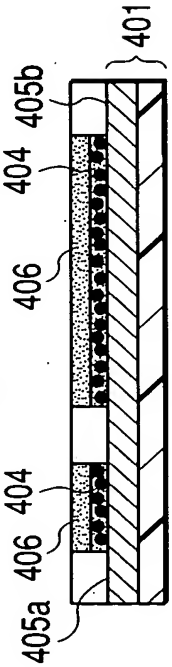


FIG. 11D

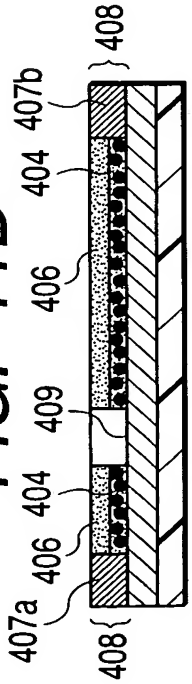


FIG. 11E

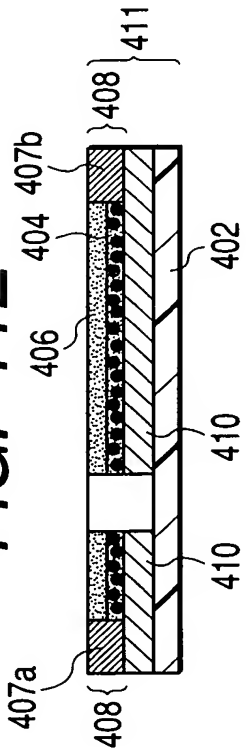


FIG. 11F

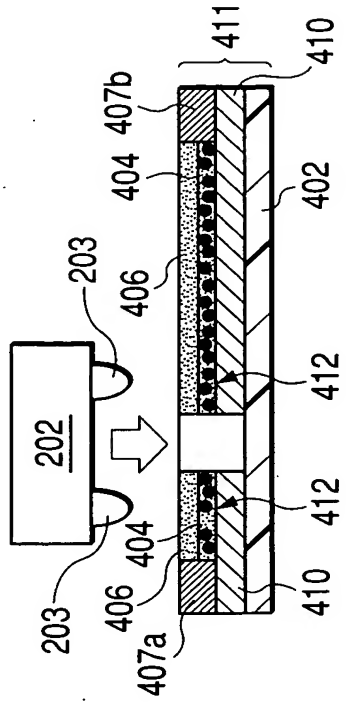


FIG. 11G

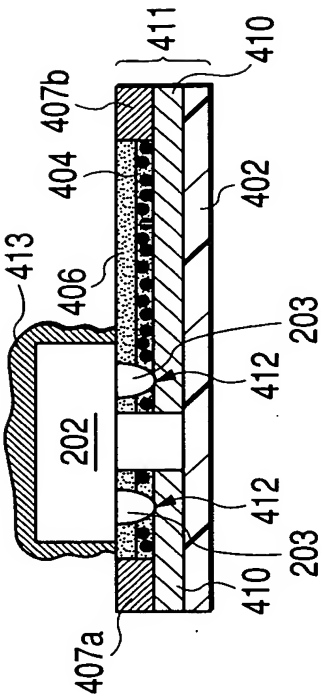


FIG. 12A

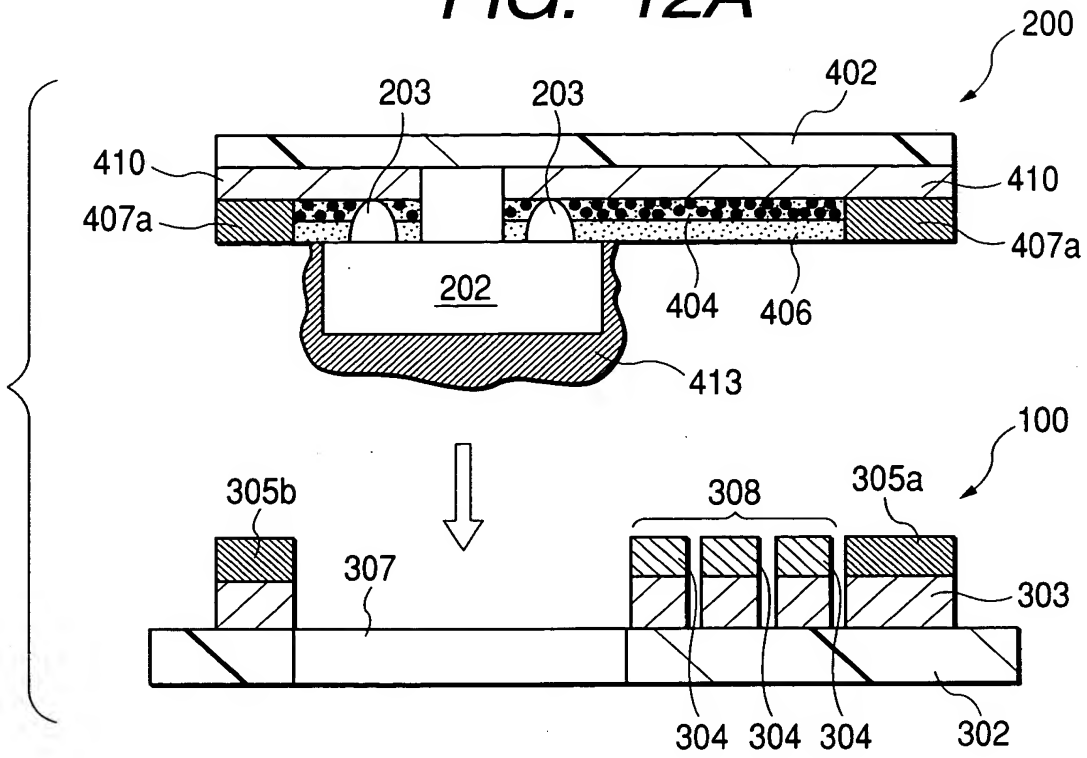


FIG. 12B

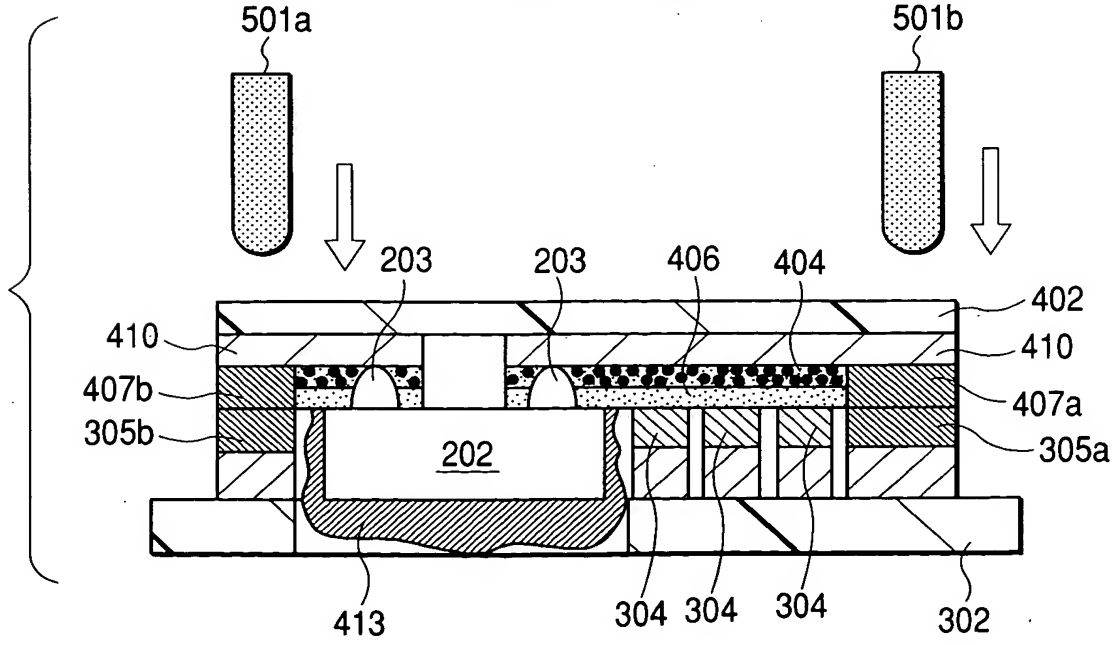


FIG. 13

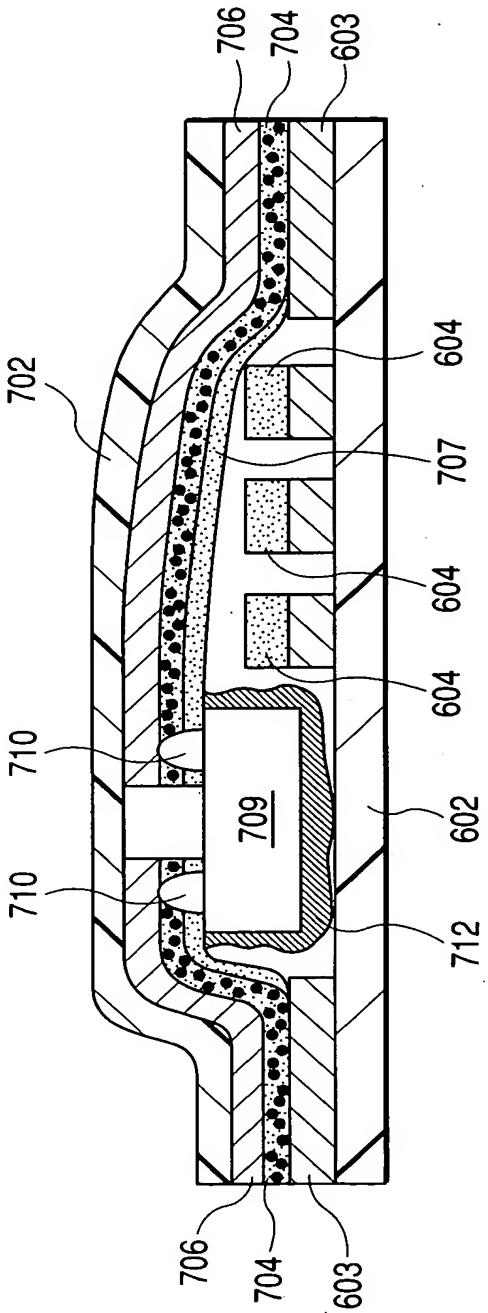


FIG. 14A

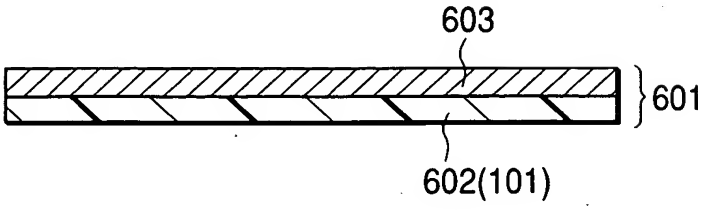


FIG. 14B

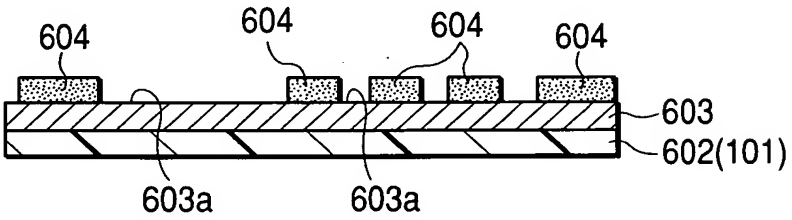
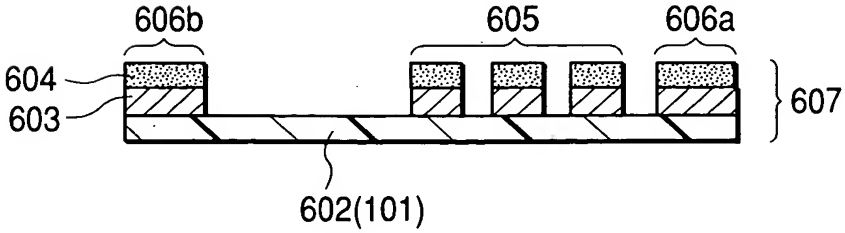


FIG. 14C



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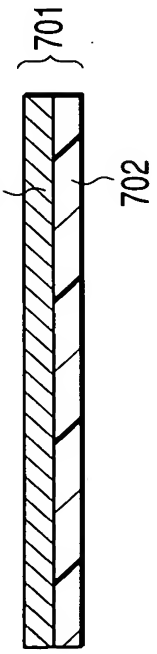

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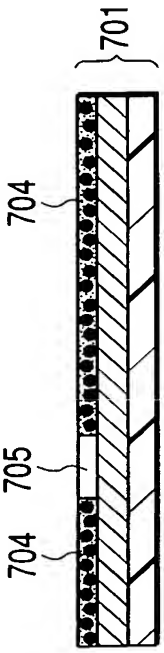

FIG. 15C

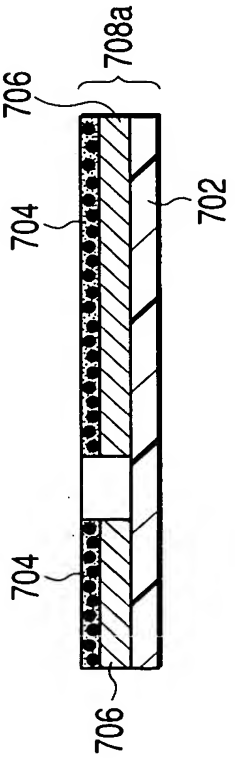

FIG. 15D

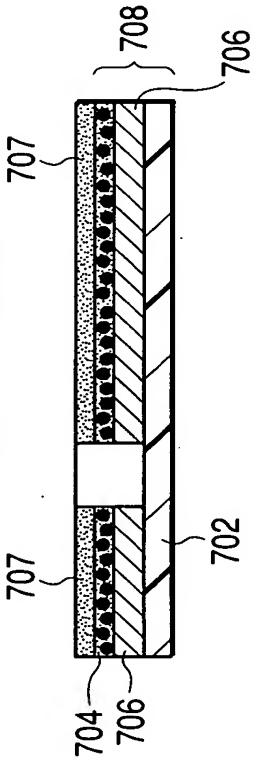

FIG. 15E

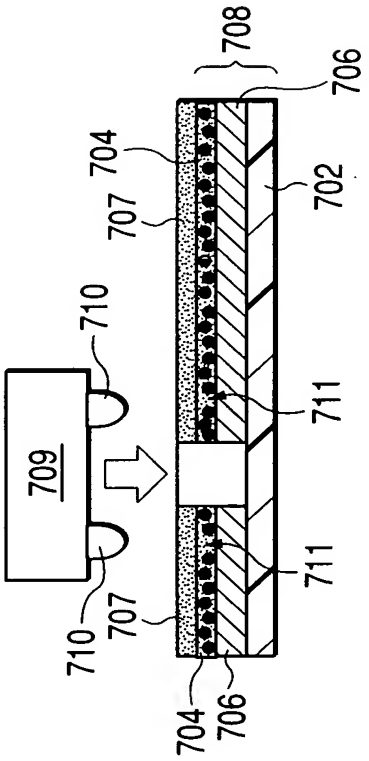

FIG. 15F

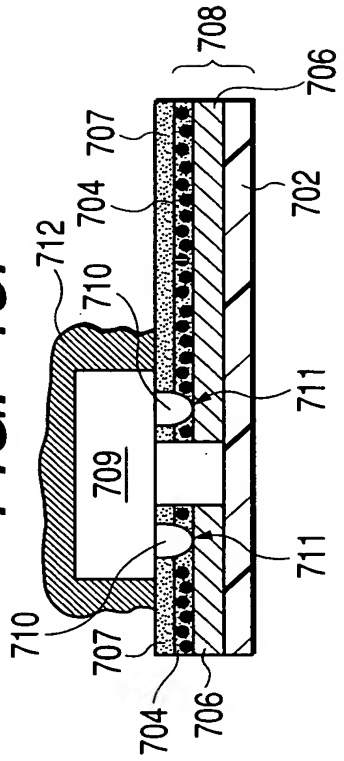

FIG. 16A

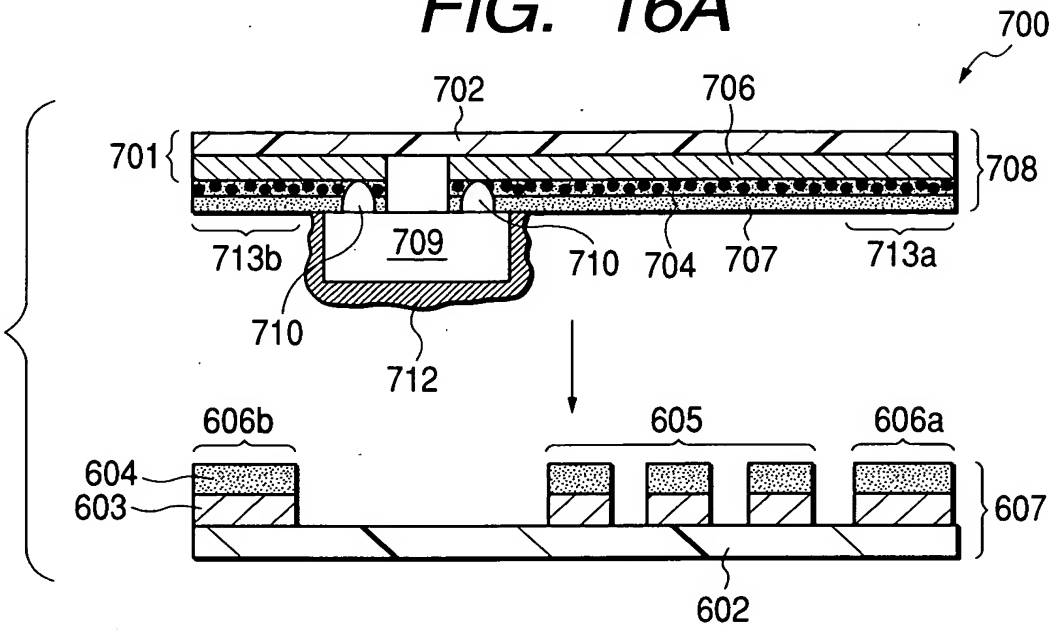

FIG. 16B

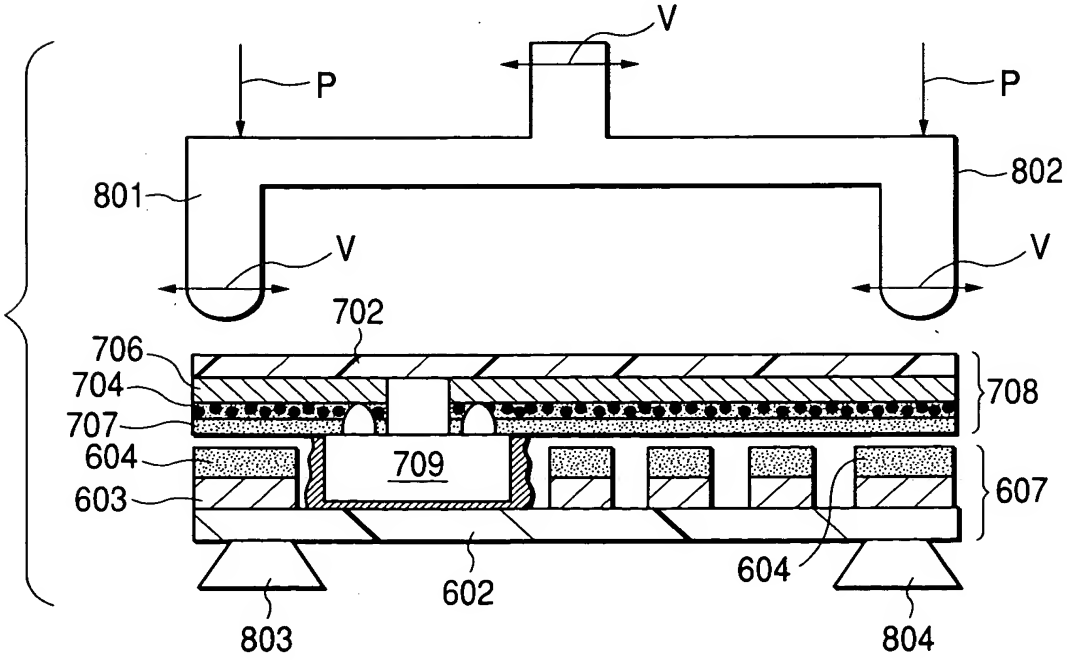

FIG. 17

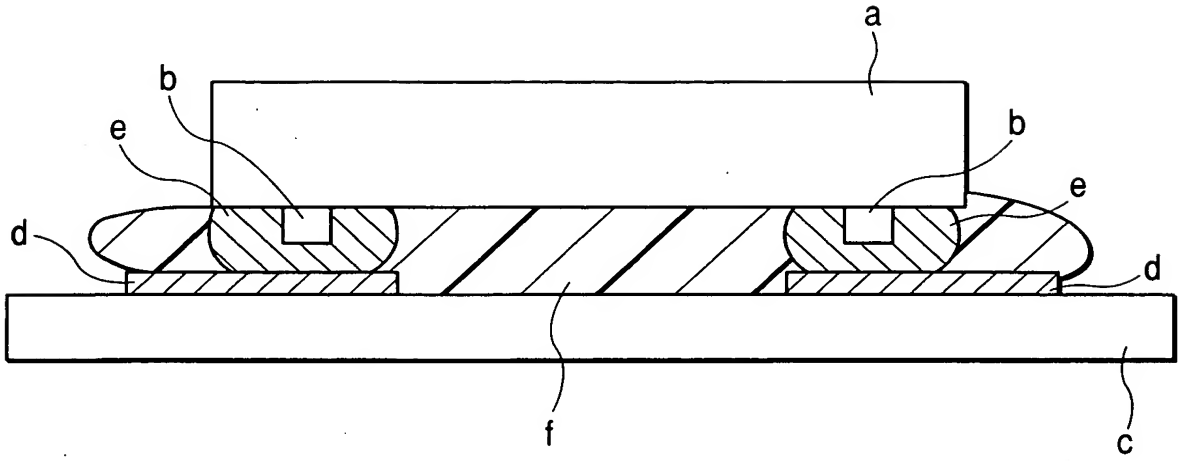

FIG. 18

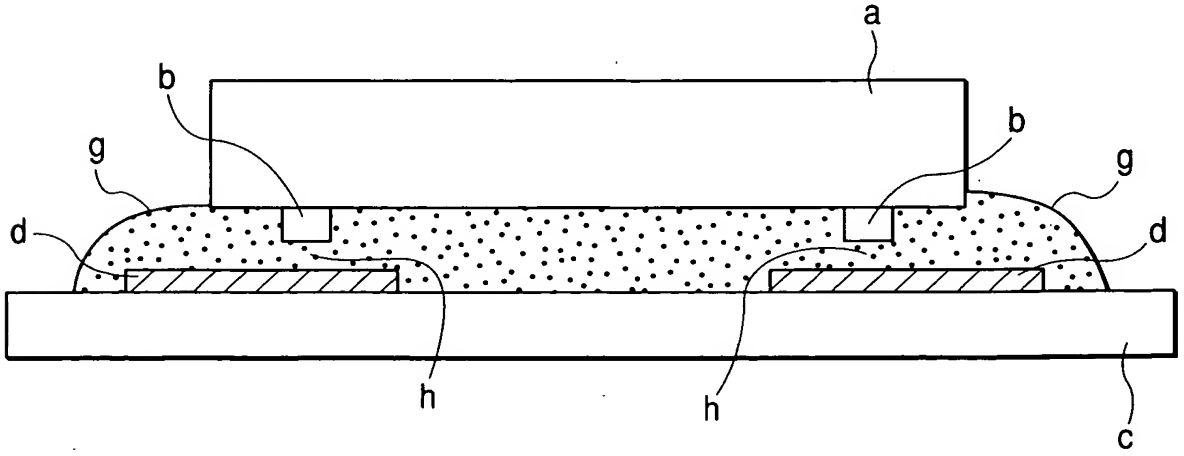

FIG. 19A

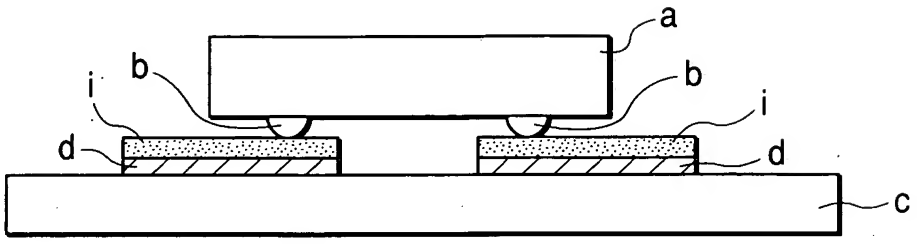

FIG. 19B

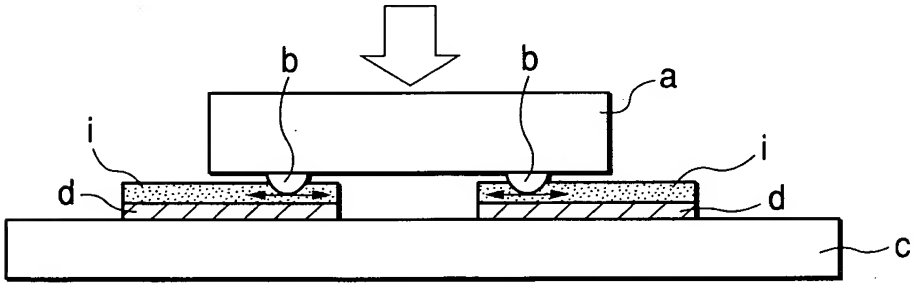

FIG. 19C

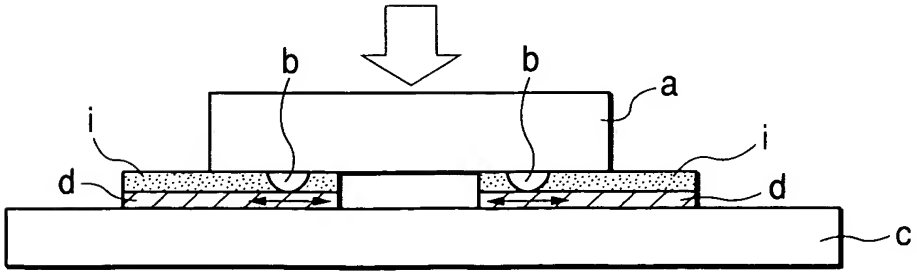

FIG. 20A

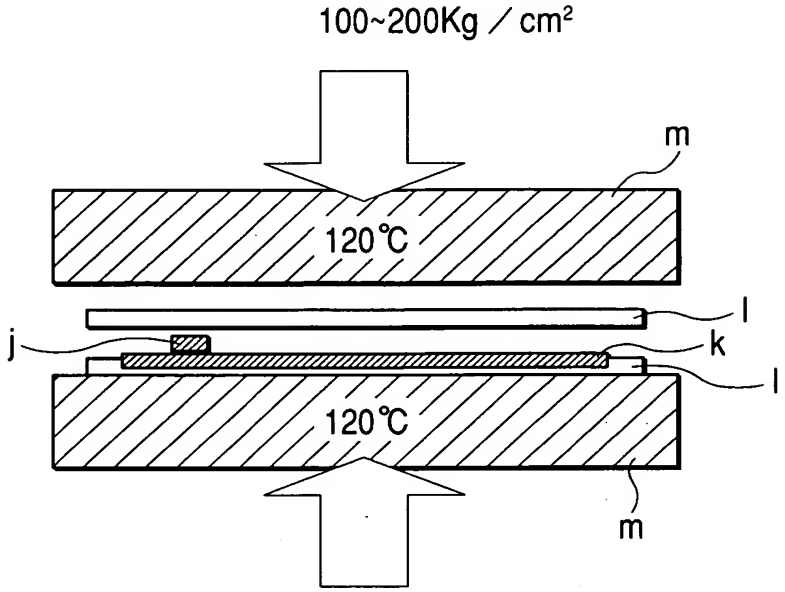

FIG. 20B

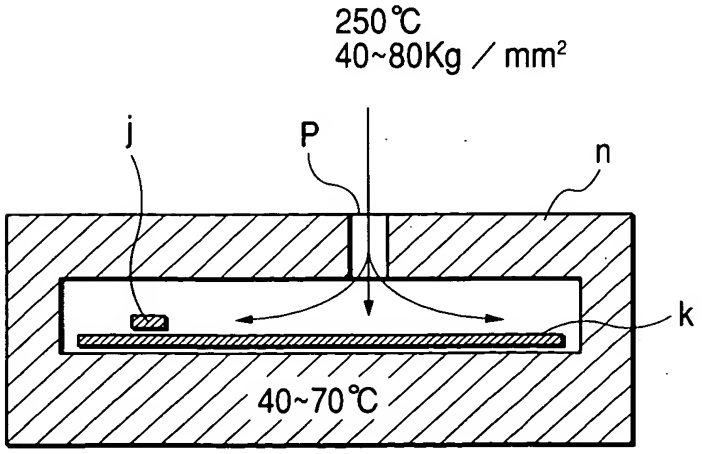

FIG. 21A

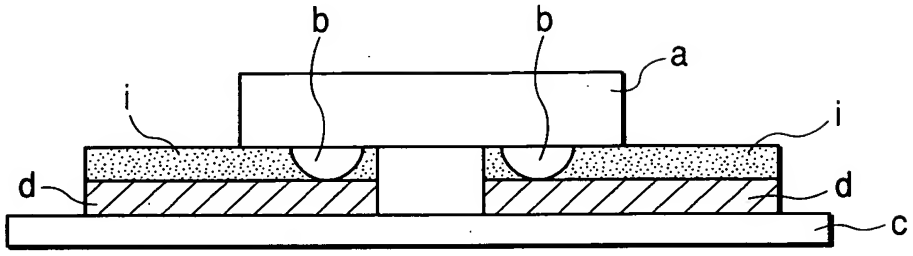

FIG. 21B